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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,156	08/31/2000	Vishnu K. Agarwal	MI22-1518	4650
21567	7590	09/01/2005	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201				NGUYEN, THANH T
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,156	AGARWAL ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 June 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 and 27-37 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-15 and 27-37 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. ____ .
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6/30/05. 5) Notice of Informal Patent Application (PTO-152)
6) Other: ____ .

DETAILED ACTION

Request for Continued Examination

The request filed on 6/30/05 for a Request for Continued Examination (RCE) under 37 CFR 1.114 is acceptable and an RCE has been established. An action on the RCE follows.

Information Disclosure Statement

The information disclosure statement filed on 6/30/05 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamanishi (U.S. Patent No. 6,307,730).

Referring to figures 3a-8J, Yamanishi teaches a method of fabricating a capacitor comprising:

Forming undoped, rugged polysilicon (HSG polycrystalline silicon 21a/31a, see col. 4, lines 14-15, figure 3c/4c) over a substrate;

Forming first capacitor electrode comprising TiN (12/32, col. 5, lines 34-36, 55-57) over the rugged polysilicon, the first electrode having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer most surface area per unit area of the substrate, the innermost surface of the first electrode comprising a surface of the first electrode that is firstly formed over the substrate, and the outermost surface of the first electrode comprising a surface of the first electrode that is lastly formed over the substrate (HSG has a larger surface area than the plain smooth substrate surface, see figures 3d-3f, 4d-4f, col. 4-6, lines 35+);

Forming a capacitor dielectric layer (14) over the first electrode; and

Forming a second capacitor electrode (15) over the dielectric layer.

Regarding to claims 2, 11, 14 the first electrode consists of TiN (12/32, col. 5, lines 34-36, 55-57).

Regarding to claim 3, wherein the substrate comprises a bulk semiconductor wafer (called monocrystalline silicon substrate, see col. 2, lines 27-29).

Regarding to claim 4, the first electrode (12/32) is on and in contact with the rugged polysilicon (21a/31a, see figure 4d-4g).

Regarding to claim 5, the rugged polysilicon comprises hemispherical grain polysilicon (called HSG-poly, see col. 4, lines 24+).

Regarding to claim 9, 15, the dielectric layer comprises Ta_2O_5 , ZrO_2 , WO_3 , Al_2O_3 , HfO_2 , barium strontium titanate, or strontium titanate (see col. 4, lines 56-67).

Regarding to claim 27, the TiN forms a continuous layer within the first electrode (see figure 3d/4d).

Regarding to claims 10, 28, referring to figures 18⁺, forming an opening in an insulative layer (21) over a substrate, the opening having sides and a bottom defined by an exposed surface of the insulative layer and having a bottom defined by an exposed surface of the substrate;

Forming a layer of polysilicon (23) over the sides and bottom of the opening;

Removing the polysilicon layer form over the bottom opening (see figure 19);

Converting at least some of the polysilicon layer undoped hemispherical grain polysilicon (23, see figure 20);

Conformally forming a continuous first capacitor electrode (24, Ru, see figure 22) on and in contact with the hemispherical grain polysilicon (23a), the first electrode being sufficiently thin (conformally along the surface of HSG wherein the HSG is not filled) that the first electrode has an outer most surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode and the outermost surface of the first electrode comprising a surface of the first electrode that is lastly formed (HSG has a larger surface area than the plain smooth substrate surface, see figure 22);

Forming a capacitor dielectric layer (26) on the first electrode; and

Forming a second capacitor electrode (27) over the dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6-8, 10-15, 27-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanishi (U.S. Patent No. 6,307,730) as applied to claims 1-5, 9 above in view of Fukuzumi et al. (U.S. Patent No. 6,222,722), Sneh et al. (U.S. Patent No. 6,551,399) and Raaijmakers et al. (U.S. Patent No. 6,780,704).

Referring to figures 3a-8J, Yamanishi teaches a method of fabricating a capacitor comprising:

Forming an opening (HL) in an insulative layer (10) over the substrate, the opening having sides and a bottom;

Forming undoped, rugged polysilicon (HSG polycrystalline silicon 21a/31a, see col. 4, lines 14-15, figure 3c/4c) over a substrate;

Forming first capacitor electrode comprising TiN (12/32, col. 5, lines 34-36, 55-57) over the rugged polysilicon, the first electrode having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer most surface area per unit area of the substrate, the innermost surface of the first electrode comprising a surface of the first electrode that is firstly formed over the substrate, and the outermost surface of the first electrode comprising a surface of the first electrode that is lastly formed over the substrate (HSG has a

larger surface area than the plain smooth substrate surface, see figures 3d-3f, 4d-4f, col. 4-6, lines 35+);

Forming a capacitor dielectric layer (14) over the first electrode; and

Forming a second capacitor electrode (15) over the dielectric layer.

Regarding to claims 2, 11, 14 the first electrode consists of TiN (12/32, col. 5, lines 34-36, 55-57).

Regarding to claim 3, wherein the substrate comprises a bulk semiconductor wafer (called monocrystalline silicon substrate, see col. 2, lines 27-29).

Regarding to claim 4, the first electrode (12/32) is on and in contact with the rugged polysilicon (21a/31a, see figure 4d-4g).

Regarding to claim 5, the rugged polysilicon comprises hemispherical grain polysilicon (called HSG-poly, see col. 4, lines 24+).

Regarding to claim 9, 15, the dielectric layer comprises Ta₂O₅, ZrO₂, WO₃, Al₂O₃, HfO₂, barium strontium titanate, or strontium titanate (see col. 4, lines 56-67).

Regarding to claim 27, the TiN forms a continuous layer within the first electrode (see figure 3d/4d).

However, the reference does not teach forming a polysilicon and convert the polysilicon to undoped HSG polysilicon, chemisorbing layer, the rugged polysilicon comprising using a seed density sufficiently small to yield at least some spaced apart grains, the outermost surface area of the first electrode is at least 30% greater than the outer surface area of the substrate.

Referring to figures 30-34, Fukuzumi et al. teaches a method of fabricating a capacitor comprising:

Forming undoped, rugged polysilicon (51) over a substrate;

Forming first capacitor electrode comprising TiN (55) over the rugged polysilicon, the first electrode having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer most surface area per unit area of the substrate, the innermost surface of the first electrode comprising a surface of the first electrode that is firstly formed over the substrate, and the outermost surface of the first electrode comprising a surface of the first electrode that is lastly formed over the substrate (HSG has a larger surface area than the plain smooth substrate surface, see figure 34, col. 16, lines 1+);

Forming a capacitor dielectric layer (53) over the first electrode; and

Forming a second capacitor electrode (54) over the dielectric layer.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form forming a polysilicon and convert the polysilicon to undoped HSG polysilicon in process of Yamanishi as taught by Fukuzumi et al. because the process would improved capacitance and the storage charge amount can be increased.

Referring to figures 1-4, Sneh et al. teaches a layer by using ALD technique of a first precursor at least one monolayer thick over a substrate (see col. 4, lines 20+);

Forming a layer by using ALD technique of a second precursor at least one monolayer thick on the first precursor layer (see col. 4, lines 20+), a chemisorption product of the first and second precursor layers being comprised by a first capacitor electrode comprising TiN (11) over the substrate.

Raaijmaker et al. teaches forming a layer by using ALD is called chemisorbing a layer (see col. 7, lines 2-32).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a chemisorbing layer of at least one monolayer thick in process of Yamanishi as taught by Sneh et al. in view of Raaijmaker et al. because the process would provide excellent step coverage.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize density of the polysilicon layer and the surface area of the electrode, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.-hydrogenated dielectric layer), discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- density of the polysilicon layer and the surface area of the electrode) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form density of the polysilicon layer and the surface area of the electrode in process of Yamanishi because discovering the optimum or workable ranges involves only routine skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See **MPEP 203.08**).



Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN